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09/692,052	10/20/2000	Atsushi Ishikawa	009683-362	5311

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EXAMINER	
VIDA, MELANIE M	

ART UNIT	PAPER NUMBER
2626	2

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/692,052	ISHIKAWA, ATSUSHI	
	Examiner	Art Unit	
	Melanie M Vida	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8-10 and 14-15* is/are rejected.

7)☒ Claim(s) *4-7,11-13 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 10/21/1999. It is noted, however, that applicant has not filed a certified copy of the 11-299437 application as required by 35 U.S.C. 119(b).

Drawings

2. **Figures 3-4** as described in the specification on page 2, lines 12-13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. **Claims 1, 8, and 14** are objected to because of the following informalities: Claims 1, 8, and 14 state the relationship between the M-valued image data and the N-valued error as, (M > N)-valued image data by error diffusion, (claim 1, lines 1-2; claim 8, lines 1-2; and claim 14, lines 1-2). Further, these claims states "correction means correcting M-valued image data of said target pixel with an N-valued error resulting from N-arization of peripheral pixels for said target pixel", (claim 1, lines 3-5; claim 8, lines 3-5; claim 14, lines 3-5). However, figures 1-2 display

that the error, EAVExy, actually has 1+8 bits applied from the error computing part (2) to the comparator (3) for comparing the image data (Ixy) that has 8 bits. The number of bits for the error and the image data fails to satisfy the relationship M>N, as disclosed in these claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. **Claims 1-7** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. **Claim 1** states "the output means outputting an N-valued error having a smaller bit number than said corrected image data by multivalued dithering on the basis of said corrected image data and said N-valued image data", (lines 9-11). The Examiner notes that claim 1 appears to be disclosing the Applicant's first embodiment as shown in figure 1 and described in the specification on pages 5-6. However, the Examiner notes that the dependent **claim 5**, which depends on claim 1 (i.e. the first embodiment) is claiming the second embodiment as shown in figure 2 and described in the specification on page 6, line 31 through page 7, line 20. The examiner finds no embodiment or motivation in the entirety of the specification and the drawings for combining the first embodiment and the second embodiment.

Claims 2-7 are rejected for depending on claim 1 and/or claim 5 above.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8, 9, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kumashiro, US-PAT-NO: 5,870,503 (hereinafter, Kumashiro). Regarding, **claim 8,** Kumashiro, as shown in figure 15, depicts the third embodiment of an image processing apparatus, a block diagram, which reads on "an image processor", (col. 9, lines 27-31). Kumashiro illustrates that the image data, f(x,y) of 8-bits long is binarized to output b(x,y) of 1-bit, which reads on "converting M-valued image data of a target pixel to N (M>N)-valued image data", (see figure 15). Further, this method employs an error diffusion matrix (97, 95), which reads on "by error diffusion, comprising:" (See figure 15). Kumashiro, as best understood from the claim language, illustrates an error correction unit (91), which reads on "correction means", for correcting the 8-bit image data f(x,y), which reads on "for correcting said M-valued image data of said target pixel" with an 8-bit error signal E(x,y) fed directly from an error diffusion matrix (95), which reads on "with an N-valued error resulting from N-arization of peripheral pixels for said target pixel and generating corrected image data", (see figure 15). Moreover, Kumashiro teaches that a binarization unit (92), which reads on "N-arization means" compares the corrected image data f ' (x, y) and a threshold value (Th=128), which reads "comparing said corrected image data with a threshold" and converting the corrected image data f ' (x,y) to a binarized output value b(x,y), which reads on "and converting said corrected image data to N-valued image data of said target pixel;", (see figure 15). A binarization error calculation means (93), which reads on "output means" outputs a

6-valued error having a smaller bit number than the 8-valued corrected image data f ' (x, y), which reads on "outputting an N-valued error having a smaller bit number than said corrected image data on the basis of said corrected image data and said N-valued image data" (See figure 15).

Regarding, **claim 9,** Kumashiro depicts a line memory (94) with an input error e(x,y), which reads on "storage means storing N-valued error output from said output means" (see figure 15).

Regarding, **claim 14,** please refer to the corresponding rejection in claim 8.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 10, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumashiro, US-PAT-NO: 5,870,503 (hereinafter, Kumashiro).

Regarding, **claim 1,** Kumashiro, as shown in figure 15, depicts the third embodiment of an image processing apparatus, a block diagram, which reads on "an image processor", (col. 9, lines 27-31). Kumashiro illustrates that the image data, f(x,y) of 8-bits long is binarized to output b(x,y) of 1-bit, which reads on "converting M-valued image data of a target pixel to N (M>N)-valued image data", (see figure 15). Further, this method employs an error diffusion matrix (97,

95), which reads on "by error diffusion, comprising:" (See figure 15). Kumashiro, as best understood from the claim language, illustrates an error correction unit (91), which reads on "correction means", for correcting the 8-bit image data f(x,y), which reads on "for correcting said M-valued image data of said target pixel" with an 8-bit error signal E(x,y) fed directly from an error diffusion matrix (95), which reads on "with an N-valued error resulting from N-arization of peripheral pixels for said target pixel and generating corrected image data", (see figure 15). Moreover, Kumashiro teaches that a binarization unit (92), which reads on "N-arization means" compares the corrected image data f ' (x, y) and a threshold value (Th=128), which reads "comparing said corrected image data with a threshold" and converting the corrected image data f ' (x,y) to a binarized output value b(x,y), which reads on "and converting said corrected image data to N-valued image data of said target pixel;", (see figure 15). A binarization error calculation means (93), which reads on "output means" outputs a 6-valued error having a smaller bit number than the 8-valued corrected image data f ' (x, y), which reads on "outputting an N-valued error having a smaller bit number than said corrected image data" (See figure 15).

Kumashiro does not expressly disclose "multivalued dithering on the basis of said corrected image data and said N-valued image data".

However, Kumashiro, as shown in figure 20, illustrates a multi-valued dither matrix (114), which reads on "multivalued dithering" (114) that is applied to the most significant bits of the image data f1, which reads on "on the basis of corrected image data" wherein the original image data was 8-bits long, which reads on "and said N-valued image data", (see figure 20).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify figure 15 to include the multi-valued dithering matrix of figure 20.

One of ordinary skill in the art would have been motivated to use a multi-value dither matrix, in order to convert an input image data of 8 bits into dither image data of 4-bits, given the express suggestion of Kumashiro, (col. 11, line 67 through col. 12, lines 1-2).

Regarding, **claim 2,** Kumashiro depicts a line memory (94) with an input error e(x,y), which reads on "storage means storing N-valued error output from said output means" (see figure 15).

Regarding, **claim 3,** Kumashiro, as shown in figure 26, illustrates a conventional system in which the average error $Eave_{xy}$ is calculated for a target pixel based on peripheral pixels of an error diffusion matrix (26) comprised of weighting values, which reads on "said correction means computes weighted error on the basis of N-valued error of said peripheral pixels for said target pixel stored" wherein the errors are stored in (25), which reads on "stored in said storage means and weighting factors", (see figure 26). The input image data f(xy) is corrected (21) based on adding the average error $Eave_{xy}$ to the input image data to form corrected image data f1(x,y), which reads on "and performs correction on the basis of said average weighted error", (see figure 26).

Regarding, **claims 10 and 15,** Kumashiro teaches the image processor of claim 8, but fails to expressly disclose, "said correction means computes an average weighted error on the basis of said N-valued error of said peripheral pixels for said target pixel stored in said storage means and weighting factors, and performs correction on the basis of said average weighted error".

However, Kumashiro in figure 26, illustrates a conventional system in which the average error $Eave_{xy}$ is calculated for a target pixel based on peripheral pixels of an error diffusion matrix

(26) comprised of weighting values, which reads on "said correction means computes weighted error on the basis of N-valued error of said peripheral pixels for said target pixel stored" wherein the errors are stored in (25), which reads on "stored in said storage means and weighting factors", (see figure 26). The input image data f(xy) is corrected (21) based on adding the average error $Eave_{xy}$ to the input image data to form corrected image data f1(x,y), which reads on "and performs correction on the basis of said average weighted error", (see figure 26).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify figure 15 to include the average weighted error calculation as in figure 26.

One of ordinary skill in the art would have been motivated to compute an average error in order to modify the input image, given the express suggestion of Kumashiro (see figure 26).

Allowable Subject Matter

7. **Claims 4-7, 11-13, and 16-18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 4-7, 11-12 and 16-18 are allowed because the prior art of record does not teach or suggest the collective features of the invention, such as in claim 4, the step of relating $n=2^n$ between the number n of bit reduction by said multivalued dithering and the sum m of said weighting factors; Claim 5 is allowed because of the multivalued dithering is performed on the corrected image data; Claim 6 is allowed because the outpu means generates N-valued error on the basis of said corrected image data subjected to multi-valued dithering of said n-valued image data; Claim 7 is allowed because multi-valued dithering is performed on the difference data between the corrected image data and the data based on N-valued image data; Claim 11 is allowed for the same reason as claim 5. Claim 12 is allowed

because of the same reason as claim 6. Claim 13 is allowed for the same reason as claim 7; Claim 16 is allowed for the same reason as claim 5. Claim 17 is allowed for the same reasons as claim 6. Claim 18 is allowed for the same reason as claim 7.

8. **Claims 4-7** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kumashiro, US-PAT-NO: 6,369,912 B1, an image processing apparatus carrying out binarization using error diffusion method.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melanie M Vida whose telephone number is (703) 306-4220. The examiner can normally be reached on 8:30 am 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott A Rogers can be reached on (703)305-4726. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Melanie M Vida
Examiner
Art Unit 2626

MMV

mmv

June 25, 2004

SCOTT ROGERS
PRIMARY EXAMINER